Electronic Version
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# Claims

[c1] 1. A method of fabricating a flash memory, comprising the steps of:
providing a substrate having a tunneling dielectric layer and a patterned mask layer sequentially formed thereon;
removing portions of the tunneling dielectric layer and the substrate using the patterned mask layer as an etching mask to form a plurality of trenches in the substrate;
depositing an insulating material into the trenches to form a plurality of device isolation structures;
forming a sacrificial material layer over the substrate, covering the patterned mask layer and the isolation structure;
patterning the sacrificial material layer for forming a plurality of sacrificial layers on the isolation structures;
removing the patterned mask layer for exposing the tunneling dielectric layer;
forming a first conductive layer over the substrate;
removing a portion of the first conductive layer to expose top sections of the sacrificial layers to form a plurality of floating gates;
removing the sacrificial layers;
forming a inter-gate dielectric layer over the substrate,

covering the floating gate;

forming a control gate over the inter-gate dielectric layer; and

forming a source region and a drain region in the substrate on each side of the control gate.

[c2] 2. The method of claim 1, wherein the material of the sacrificial layer and the first conductive layer have different etching selectivities.

[c3] 3. The method of claim 2, wherein material constituting the sacrificial layer comprises silicon nitride.

[c4] 4. The method of claim 1, wherein the step for removing a portion of the first conductive layer to expose the top sections of the sacrificial layers comprises performing a chemical-mechanical polishing operation.

[c5] 5. The method of claim 1, wherein the sacrificial layer and the patterned mask layer are form by identical material so that the patterned mask layer is also removed in the process of patterning the sacrificial material layer.

[c6] 6. The method of claim 5, the material of the sacrificial layer and the patterned mask layer comprises silicon nitride.

[c7] 7. The method claim 1, wherein the material of the first

conductive layer comprises doped polysilicon.

[c8] 8. The method of claim 1, further comprising forming a second conductive layer between the tunneling dielectric layer and the patterned mask layer, and the second conductive layer is exposed after the patterned mask layer is removed.

[c9] 9. The method of claim 8, further comprising removing the second conductive layer after removing the patterned mask layer.

[c10] 10. The method claim 8, wherein the material of the second conductive layer comprises doped polysilicon.

[c11] 11. A method of fabricating a floating gate, comprising the steps of:
providing a substrate having a plurality of device isolation structures for defining an active region and a tunneling oxide layer and a patterned mask layer sequentially formed within the active region over the substrate;
forming a sacrificial layer on the substrate;
performing a lithographic-etching process for retaining the sacrificial layer on the isolation structures;
removing the patterned mask layer for exposing the tunneling dielectric layer;
forming a first conductive layer over the substrate;

removing a portion of the first conductive layer until exposing a top of the sacrificial layer; and
removing the sacrificial layer.

[c12] 12. The method of claim 11, wherein the material of the sacrificial layer and the first conductive layer have different etching selectivities.

[c13] 13. The method of claim 12, wherein the material of the sacrificial layer comprises silicon nitride.

[c14] 14. The method of claim 11, wherein the step for removing a portion of the first conductive layer to expose the top section of the sacrificial layer comprises performing a chemical-mechanical polishing operation.

[c15] 15. The method of claim 11, wherein the sacrificial layer and the patterned mask layer are formed by identical material so that the patterned mask layer is also removed in the process of patterning the sacrificial material layer.

[c16] 16. The method of claim 15, the material of the sacrificial layer and the patterned mask layer comprises silicon nitride.

[c17] 17. The method claim 11, wherein the material of the first conductive layer comprises doped polysilicon.

[c18] 18. The method of claim 11, further comprising forming a second conductive layer between the tunneling dielectric layer and the patterned mask layer, and the second conductive layer is exposed after the patterned mask layer is removed.

[c19] 19. The method of claim 18, further comprising removing the second conductive layer after removing the patterned mask layer.

[c20] 20. The method claim 18, wherein the material of the second conductive layer comprises doped polysilicon.